IN THE DRAWINGS:

The attached sheet of drawings includes changes to FIG. 7. This sheet, which includes FIGS. 7-8, replaces the original sheet including FIGS. 7-8.

REMARKS

Claims 1-2, 4-9 and 11-21 are pending in this application, of which claims 1, 4-7, 11-14 and 17-21 have been amended. Claims 3 and 10 have been canceled. No new claims have been added.

The Examiner has objected to the drawings for failing to show the second drive signal (SG12) having a pulse width greater than the first drive signal (SG11). Accordingly, FIG. 7 has been corrected to show that the pulse widths of S14 and SG11 are the same, and the pulse widths of S15 and SG12 are the same, where the pulse width of S15/SG12 is greater than the pulse width of S14/SG11.

The claims stand rejected as follows:

(1) Claims 1, 2, 7, 14, 15 and 21 under 35 U.S.C. § 103(a) as unpatentable over **Bazinet et al.** (previously applied) in view of U.S. Patent 6,288,524 to Tsujimoto (hereafter, "**Tsujimoto**");

(2) Claims 3, 8-10, 16 and 20 under 35 U.S.C. § 103(a) as unpatentable over **Bazinet et al.** in view of **Nishimaki** (previously applied) and further in view of **Tsujimoto**;

(3) Claims 4, 11 and 17 under 35 U.S.C. § 103(a) as unpatentable over **Bazinet et al.**, **Nishimaki**, **Tsujimoto** and **Bridge** (previously applied);

(4) Claims 5, 12 and 18 under 35 U.S.C. § 103(a) as unpatentable over **Bazinet et al.**, **Nishimaki**, **Tsujimoto** and **Matsuda** (previously applied); and

(5) Claims 6, 13 and 19 under 35 U.S.C. § 103(a) as unpatentable over **Bazinet et al.**, **Nishimaki**, and **Tsujimoto** in view of U.S. Patent 6,577,517 to Jain et al. (hereafter, "**Jain et al.**").

Applicants respectfully traverse these rejections.

As noted in the Preliminary Amendment filed April 3, 2006, **Bazinet et al.** fails to disclose generating the second drive signal (SG12) having a pulse width greater than that of the first drive signal (SG11) when the first drive signal is supplied to the main switching element (3). **Bazinet et al.** provides an L level second drive signal (116, 124) having the same pulse width as that of an H level first drive signal (118, 126) to the synchronous switching element (14) when the first drive signal (118, 126) is supplied to the main switching element (12) (see FIGS. 3 and 4 of **Bazinet et al.**).

The Examiner has admitted that **Bazinet et al.** does not disclose the second drive signal having a pulse width greater than that of the first drive signal, but he has cited **Tsujimoto** for teaching this feature.

Applicants respectfully disagree. **Tsujimoto** discloses a DC/DC converter and a controlling circuit thereof. A pair of switches is alternately turned on or off according to a state of a flip-flop. The flip-flop is set according to a set pulse which is periodically generated by an oscillator, and is reset according to a reset signal output from a comparator. The comparator generates a reset signal when the inductor current signal representing an inductor current becomes larger than the current instruction signal determined based on an output voltage. An

offset generating circuit provides an offset to the inductor current signal while a switch is OFF.

Combining the teachings of **Tsujimoto**, which shows a longer duration for the M2 driving signal than the M1 driving signal, with those of **Bazinet et al.** would destroy the synchronous operation of **Bazinet et al.**, in which the on-off timings of PWM command signal G2, gate drive signal 40 and gate drive signal 38 are all synchronized so that all pulses are the same length, as shown in FIGS. 3 and 4 of **Bazinet et al.** Thus, these references are not properly combinable to teach the present invention.

Bazinet et al. fails to disclose generating a first drive signal by delaying a pulse signal, generating a delayed signal by delaying the first drive signal, and generating a second drive signal by synthesizing the pulse signal with the delayed signal, as recited in claims 3 and 10 of the instant application. Accordingly, claims 3 and 10 have been cancelled and their limitations added to claims 1, 7, 14 and 21.

Thus, the 35 U.S.C. § 103(a) rejection of claims 1, 2, 7, 14, 15 and 21 should be withdrawn.

Nishimaki has a U.S. filing date of July 22, 2003, which is subsequent to the foreign priority date of August 22, 2002 claimed in the instant application. Thus, **Nishimaki** is not a proper §103(a) reference, and all of the 35 U.S.C. §103(a) prior art rejections based on **Nishimaki** should be withdrawn.

In view of the aforementioned remarks, claims 1-2. 4-9 and 11-21, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Petition for Extension of Time
Replacement Sheets of Drawing (FIGS. 7and 8)
Check in the amount of $120.00
English Translation of Japanese Application. No. 2002-242422

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